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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,582	01/25/2000	Tatsushi Inagaki	JA998-218	7320

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EXAMINER	
HOANG, PHUONG N	
ART UNIT	**PAPER NUMBER**
2126	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/490,582	INAGAKI ET AL.	
	Examiner	Art Unit	
	Phuong N. Hoang	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,14, and 21* is/are allowed.

6)☒ Claim(s) *1 - 6, 8 - 13, and 15 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 21 are pending for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1 – 6, 8 – 13, and 15 – 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

a. As to claim 1, examiner did not see anywhere in the specification describing the digital data objects, and digital data processing device. For examiner purpose, examiner pressed "digital" to mean the digit of the flag bit being 00 or 01.

b. As to claims 8 and 15, they are program and system claims of claim 1. They are rejected as the same reason above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 4, 6, 8 – 11, 13, 15 – 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cierniak "Briki: an Optimizing Java Compiler" pages 179 – 184 in view of Hastings, US patent no. 5,835,701.

6. **As to claim 1**, Ciermiak teaches a method for processing a multidimensional array object comprising array objects, said multidimensional array object and said array objects being digital data objects storable in addressable data storage locations of a digital data processing device, said method comprising the steps of:

accessing flags (access flags, page 180, section 2.2), said multidimensional array object (multi-dimensional array, abstract and section 4, and 4.1), a defined set of instructions (many instructions, section 5.3) executable by a data processing device;

executing a machine code (machine code, abstract and section 3) performing said process, said machine code being selected from among a plurality of machine codes (set of machine-dependent and high-level optimizations, abstract and section 3) performing said process .

Cierniak teaches that the process is optimized when the multidimensional array is allocated in consecutive memory locations (section 4.1 and 4.2).

Cierniak does not explicitly teach the step of the flags representing whether it is possible to optimize a process for elements of said multidimensional array object.

Hastings teaches the step of state of flag showing the memory allocation (status bits = 00, col. 9 lines 15 – 40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Cierniak and Hasting's system because Hasting's state of the flag would provide a signal to the system that when the multi-dimensional array is allocated in the consecutive memory locations to enable the accessing and to optimize the execution times.

7. **As to claim 2**, Cierneak modified by Hasting teaches the step of inverting the flags (Hasting; status bit changes, col. 9 lines 15 – 40) when a predetermined condition (when multi-dimensional array is allocated in the consecutive memory locations, sections 4.1 and 4.2) is no longer met.

As to claim 3, Cierneak teaches the step of accessing flags (access flags, page 180, section 2.2), optimize (section 4.1 and 4.2) a process for elements of the multidimensional array object (optimization the multi-dimensional arrays, abstract and section 4, 4.1, and 4.1), wherein the predetermined condition is whether a base array of a multidimensional array object is allocated to consecutive memory area (the array-

based multi-dimensional arrays is optimized when they are placed in consecutive memory area, section 4.1, 4.2, and 5.3).

Cierniak does not explicitly teach the step of the flags representing whether it is possible to optimize a process for elements of said multidimensional array object, and inverting flags.

Hastings teaches the step of state of flag showing the memory allocation (status bits = 00, col. 9 lines 15 – 40), inverting the flags (status bits change, col. 9 lines 15 – 40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Cierniak and Hasting's system because Hasting's state of the flag would provide a signal to the system that when the multi-dimensional array is allocated in the consecutive memory locations to enable the accessing and to optimize the execution times.

8. **As to claim 4**, Cierneak teaches the step of wherein the machine code is either a machine code optimized or a machine code not optimized according to the predetermined condition (simple access .... Instructions, section 5.3)

9. **As to claim 6**, Ciernark teaches the step of if the predetermined condition is met when generating the multidimensional array object, setting the flags to a generated multidimensional array object (if fields to be access ... in consecutive memory locations, section 4.2).

10. **As to claim 8**, this is the program claim of claim 1. See rejection for claim 1 above.

11. **As to claim 9,** see rejection for claim 2 above.

12. **As to claim 10**, this is the product claim of claim 3. See rejection for claim 3 above.

13. **As to claim 11**, see rejection for claim 4 above.

14. **As to claim 13**, see rejection for claim 6 above.

15. **As to claim 15**, this is the system claim of claim 1. See rejection for claim 1 above.

16. **As to claim 16**, see rejection for claim 2 above.

17. **As to claim 17**, this is the system claim of claim 3. See rejection for claim 3 above.

18. **As to claim 18**, see rejection for claim 4 above.

19. **As to claim 20**, see rejection for claim 6 above.

20. Claims 5, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cierniak "Briki: an Optimizing Java Compiler" pages 179 – 184 in view of Hastings, US patent no. 5,835,701, and further in view of Wolczko, US patent no. 6,15,782.

21. **As to claim 5**, Cierniak and Hasting do not explicitly teaches the step of determining whether the predetermined condition is met when writing to the array.

Wolczko teaches the step of writing to the array (optimized .... Write-barrier, col. 8 lines 50 – 64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Cierniak, Hasting, and Woczko's system because Woczko's writing to the array would provide the significant time access and therefore need to speed up the system.

22. **As to claim 12**, see rejection for claim 5 above.

23. **As to claim 19**, see rejection for claim 5 above.

Response to Arguments

24. Applicant's arguments with respect to claims 1 – 6, 8 – 13, and 15 - 20 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

25. Claims 7, 14, and 21 are allowed.

Conclusion

26. The prior art made of record but not relied upon request is considered to be pertinent to applicant's disclosure.

Austin, US patent no. 5,644,709, demonstrating the method of optimizing memory access.

Sibley, "A definition optimization technique used in a code translation algorithm", demonstrating the data flow analysis of using the flag to optimize the program.

Magerman, US patent no. 5,214,599, demonstrating a multi-dimensional array having an inverted.

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong N. Hoang whose telephone number is (571)272-3763. The examiner can normally be reached on Monday - Friday 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ph
December 3, 2004

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